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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/777,097
Filing Date: February 13, 2004
Appellant(s): MOON ET AL.

Seok-Won Stuart Lee
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 4/20/07 appealing from the Office action mailed 8/18/06.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,307,007	Wu et al.	4-1994
5,180,967	Yamazaki	1-1993

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 3 and 5-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Wu et al. (USPN 5,307,007).

Fig. 1 discloses a bias circuit part M1-M4 & R1, an output node (node between M1 & M3), a start-up capacitor C1, a common node (gates of M1/M2) and MOS transistors M1/M2 as recited in claim 1.

Fig. 3 discloses a bias circuit M1-M8 & R1, an output node (node between M5 & M7, a first common node (gates of M3/M4), first MOS transistors M3 & M4, a second common node (gates of M5/M6), second MOS transistors M5 & M6, a fist capacitor C1 and a second capacitor C2 as recited in claim 3.

The output node outputs the constant bias voltage to another circuit outside the bias circuit (wherein M5 and M6 are seen as the another circuit outside the bias circuit) as recited in new claims 5 and 7.

The output node outputs the constant bias voltage to another circuit outside the bias circuit (wherein M9 and M10 are seen as the another circuit outside the bias circuit) as recited in new claims 6 and 8.

Claim 9 is seen to be the same as claim 1 wherein "output node" has been replaced with "output terminal" and "base of the output terminal". No patentable difference is seen to exist between these three phrases. Claim 9 is anticipated for the reasons above.

Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki (5,180,967) in view of Wu et al. (5,307,007).

Yamazaki Fig. 1 discloses a bias circuit part 104/106/110/112/114, an output node (N11 or N12), a common node (gates of 104/106) and MOS transistors 104/106 as recited in claim 1. Further shown are start-up circuits 118 & 120. Not shown is a start-up capacitor as recited in claim 1. As indicated in the 102 rejections above, Wu et al. Fig. 1 (as well as Figs. 2, 4 & 6) disclose similar bias circuit parts including an output node, a common node and MOS transistors as well as start up capacitors C1 and C2. It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the Yamazaki start-up circuits 118 & 120 with a start-up capacitor as taught by

Wu et al. for the benefit of reducing component count and static current consumption. Claim 1 is obvious.

Yamazaki Fig. 1 further discloses a first PMOS 106, a second PMOS 104, a first NMOS 110, a second NMOS 112 and a resistor 114 as recited in claim 2. Both N11 and N12 are valid output nodes. Yamazaki extracts a signal from the output node between the second PMOS transistor 104 and the second NMOS transistor 112, however, Wu et al. Fig. 1 shows that a signal can just as well be extracted from the output node between the first PMOS transistor M1 and the first NMOS transistor M3. Claim 2 is obvious.

Yamazaki Fig. 5 discloses a bias circuit 104/106/124/126/130/128/114, an output node (nodes between 126 & 110 or between 124 &112), first MOS transistors 104 & 106 and second MOS transistors 124 & 126 as recited in claim 3. Further shown are start-up circuits 118 & 120. Not shown are start-up capacitors as recited in claim 3. As indicated in the 102 rejections above, Wu et al. Fig. 3 (as well as Fig. 5) disclose similar bias circuits including an output node, and MOS transistors as well as start up capacitors C1 and C2. It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the Yamazaki start-up circuits 118 & 120 with start-up capacitors as taught by Wu et al. for the benefit of reducing static current consumption. Claim 3 is obvious.

Yamazaki Fig. 5 further discloses a first PMOS 106, a second PMOS 104, a third PMOS 126, a fourth PMOS 124, a first NMOS 110, a second NMOS 112 and a resistor 114 as recited in claim 4. Nodes between 126 & 110 or between 124 &112 are all valid

output nodes. For example, Wu et al. Fig. 3 shows that a signal can be extracted from an output node formed by the drain of the first NMOS transistor M7. Claim 4 is obvious.

The output node outputs the constant bias voltage to another circuit outside the bias circuit (wherein 116 (or M5 and M6 from Wu et al.) are seen as the another circuit outside the bias circuit) as recited in new claims 5 and 7.

The output node outputs the constant bias voltage to another circuit outside the bias circuit (wherein 116 (or M9 and M10 from Wu et al.) are seen as the another circuit outside the bias circuit) as recited in new claims 6 and 8.

New claims 9 and 10 are seen to be the same as existing claims 1 and 2 wherein "output node" has been replaced with "output terminal" and "base of the output terminal". No patentable difference is seen to exist between these three phrases. Claims 9 and 10 are obvious for the reasons above.

(10) Response to Argument

Beginning at the bottom of page 11 of the Appeal Brief, Appellants argue that the relied upon Wu et al. reference does not show an "output node" as recited in claim 1. Examiner initially notes that the output node between M1 and M3 (Wu et al., Fig. 1) is not connected to the gate of M1 or the source/drain of M4 as is incorrectly stated at the bottom of page 11 and top of page 12. Also, gates do not provide outputs. The source/drain connection between M1 and M3 is from where a constant bias voltage is output. Examiner never suggested that the gate of M3 provides an output signal. The gate of M3 is connected to the output node merely as a consequence of the circuit's

structure. Appellant's own Fig. 7 shows the exact same configuration at the gate of MN73.

In any event, as pointed out in the rejection above, Wu et al. Fig. 1 is seen to show an "output node" at the connection of transistors M1 and M3. This connection is called a node. The node connection between transistors M1 and M3 provides or outputs a constant bias voltage signal that is extracted by the gates of transistors M5 and M6, for example. Those of ordinary skill in the art would reasonably refer to such a connection configuration as an "output node".

Claim 1 is directed toward Appellant's Fig. 7, for example. Fig. 7 shows a slightly modified version of a well-known Wilson-type bias circuit as illustrated by Appellant's Prior Art Fig. 1. By itself, a bias circuit has no real-world value. Bias circuits are building-blocks that are used to create larger, usable electronic systems. One of ordinary skill in the art would recognize that the very purpose of a bias circuit is to provide or output a bias for extraction by another down-stream electronic component. The Wu et al. reference shows an example of a larger electronic system utilizing a Wilson-type bias circuit building-block for providing or outputting a constant bias voltage to down-stream components M5 and M6, for example. Although the node between M1 and M3 is internal to the larger electronic system, the node is, nevertheless, an output node of the Wilson-type bias sub-circuit. The output node between bias circuit transistors M1 and M3 is exactly the same as the output node REF or Vgn shown in Appellant's Fig. 1 or 7, respectively.

Finally, examiner's rejection clearly addresses the "common node" and "output node" limitations of the claim. As pointed out above, Wu et al. Fig. 1 discloses an output node (node between M1, M3 & M4) and a common node (node between M1, M2 & M4). Again, this is the exact structure shown in Appellant's Fig. 7.

In the middle of page 13 of the Appeal Brief, Appellants argue that Wu et al. Fig. 1 show an output Vout that is not located at the gate of M3. The Wilson-type bias sub-circuit comprising M1-M4, C1 & R1 is the subject of the rejection. As pointed out above, the node between M1 & M3 is an "output node" of the Wilson-type bias sub-circuit. Vout is irrelevant.

Near the bottom of page 13 of the Appeal Brief, Appellants submit that claims 3 and 9 are patentable for reasons similar to those submitted for claim 1. As pointed out in the rejections, no patentable difference is seen between the phrases "output node" and "output terminal node". Appellant's disclosure supports no alternate interpretation. Otherwise, Examiner's response as described above is the same for all of claims 1, 3 and 9. Appellant further submits that dependent claims 5-8 are allowable because their respective base claims 1 and 3 are allowable. As pointed out above, claims 1 and 3 are not allowable.

Beginning at the top of page 14 of the Appeal Brief, Appellants argue that Yamazaki Fig. 1 does not show an "output node". As pointed out in the rejection, Yamazaki Fig. 1 is seen to have an "output node" at N11 or N12. Yamazaki Fig. 1 is seen to show an "output node" at N11. This connection is called a node. The node

connection at N11 provides or outputs a constant bias voltage signal that is extracted by the gate of transistor 116. Those of ordinary skill in the art would reasonably refer to such a connection configuration as an "output node".

Again, claim 1 is directed toward Appellant's Fig. 7, for example. Fig. 7 shows a slightly modified version of a well-known Wilson-type bias circuit as illustrated by Appellant's Prior Art Fig. 1. By itself, a bias circuit has no real-world value. Bias circuits are building-blocks that are used to create larger, usable electronic systems. One of ordinary skill in the art would recognize that the very purpose of a bias circuit is to provide or output a bias to another down-stream electronic component. The Yamazaki reference shows an example of a larger electronic system utilizing a Wilson-type bias circuit building-block for providing or outputting a constant bias voltage to down-stream component 116, for example. Although the node N11 is internal to the larger electronic system, the node is, nevertheless, an output node of the Wilson-type bias sub-circuit.

On the other hand, a node is not required to provide a signal to another component to be considered an "output node". If a usable signal is available at a node, than that node is an "output node". Consequently, node N12 is also seen as an "output node". See Wu et al. Fig. 1 or Appellant's Prior Art Fig. 1, for example. The Prior Art demonstrates that a constant bias voltage is generated at each of output nodes N11 and N12 due to the symmetrical nature of the circuit. Examiner notes that Appellant's disclosure suggests no particular use or application for the constant bias voltage generated at the claimed "output node". Node N12 is exactly the same as the output

node REF or Vgn shown in Appellant's Fig. 1 or 7, respectively. Node N12 is as much an "output node" as is Appellant's REF or Vgn.

Beginning at the bottom of page 14 of the Appeal Brief, Appellants argue that Examiner has relied upon improper hindsight. In comparing the circuits of Yamazaki Fig. 1 and Wu et al. Fig. 1, for example, both references show similar bias circuit parts. Yamazaki shows start-up transistors 118 and 120 whereas Wu et al. show a start-up capacitor. One of ordinary skill in the art would readily recognize the advantage of the start-up capacitor in that component count is reduced and static current consumption is reduced or eliminated. Those of ordinary skill in the art are intuitively motivated to reduce component count and static current consumption in the pursuit of more efficient circuit designs. Such is not seen as improper hindsight. Additionally, Examiner's motivation differs from that discussed in Appellant's disclosure.

Beginning at the top of page 15, Appellant argues that Yamazaki may not generate a constant bias voltage. The portion of Appellant's circuit structure relevant to generating a constant bias voltage is identical to Yamazaki's structure relavant to generating a constant bias voltage. If Appellant's structure generates a constant bias voltage than the corresponding structure of the Yamazaki circuit must also generate a constant bias voltage. Appellant argues that Yamazaki may not offer an improvement to bias stability. Such is not claimed and is irrelevant to Examiner's combination.

On page 15 of the Appeal Brief, Appellants submit that claims 3 and 9 are patentable for reasons similar to those submitted for claim 1. As pointed out in the rejections, no patentable difference is seen between the phrases "output node" and

"output terminal node". Appellant's disclosure supports no alternate interpretation. Otherwise, Examiner's response as described above is the same for all of claims 1, 3 and 9. Appellant further submits that dependent claims 2, 4-8 and 10 are allowable because their respective base claims 1, 3 and 9 are allowable. As pointed out above, claims 1, 3 and 9 are not allowable.

Beginning near the bottom of page 15 of the Appeal Brief, Appellants argue that claim 4 cannot be rejected in view of Yamazaki Fig. 5 because of intervening components 130 and 128. This is a newly presented argument. Examiner is giving the broadest reasonable interpretation to the word "connected". Claim 4 does not require a direct connection between the drain of the first NMOS transistor 110 and the drain of the third PMOS transistor 126. Yamazaki Fig. 5 shows the drain of the first NMOS transistor 110 "connected" (via transistor 128) to the drain of the third PMOS transistor 126. The claim does not preclude the existence of transistor 128. Likewise, claim 4 does not require a direct connection between the drain of the second NMOS transistor 112 and the drain of the fourth PMOS transistor 124. Yamazaki Fig. 5 shows the drain of the second NMOS transistor 112 "connected" (via transistor 130) to the drain of the fourth PMOS transistor 124. The claim does not preclude the existence of transistor 130.

On page 17 of the Appeal Brief, Appellants submit that claim 10 is patentable for reasons similar to those submitted for claim 4. Examiner's response as described above is the same for both claims 4 and 10.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Jeffrey Zweizig

Conferees:

David Blum

Drew Richards